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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,310	09/09/2004	Hung-En Tai	LKSP0051USA	5309

27765 7590 10/19/2007

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EXAMINER	
CHAWAN, SHEELA C	

ART UNIT	PAPER NUMBER
2624	

NOTIFICATION DATE	DELIVERY MODE
10/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
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Office Action Summary	Application No.	Applicant(s)	
	10/711,310	TAI ET AL.	
	Examiner	Art Unit	
	Sheela C. Chawan	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 6/30/05, the information disclosure statement is being considered by the examiner.

Drawings

3. The Examiner has approved drawings filed on 9/9/04.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, are rejected under 35 U.S.C. 102(e) as being anticpated by Dor et al., (US. 6,744,266 B2).

As to claim 1, Dor discloses a method for managing wafer defects comprising: performing an inspection step to inspect defects on each chip of each wafer and generating corresponding wafer defect raw data; performing a data pre-treatment step with a server to integrate the wafer defect raw data according to each chip of the same wafer and generate wafer defect distribution data for recording position, type, and size of defect; performing a drawing pre-treatment step with the server to generate a corresponding drawing file according to a new position, type, and size of a defect after the wafer defect distribution data is transferred integrally to display each distribution mode of each defect on the wafer on a screen; and performing a network management step to transmit the drawing file to a terminal without receiving the wafer defect raw data at the terminal such that a terminal user is capable of seeing the defect distributions of each chip of the wafer according to the drawing file on the drawing screen (column 2, lines 51-67, column 3, lines 1-16, column 5, lines 14-18).

As to claim 2, Dor discloses the method of claim 1, wherein the wafer defect raw data records a position of a wafer defect relative to a chip grid, and the data pre-treatment step transfers the position of the wafer defect to a position corresponding to the origin of the wafer to make the wafer defect distribution data record the position of the wafer defect relative to the origin (column 6, lines 56-67).

As to claim 3, Dor discloses the method of claim 1, wherein the size of the drawing file generated by the server is smaller than the sum of all wafer defect raw data corresponding to a wafer (note, wafer data raw data is usually large because the defects are several types therefore, the drawing file, which is for one chip in its correct

form has to be only one there are several types of defects which makes the defects file to be large).

As to claim 4, Dor discloses the method of claim 1, wherein the drawing file generated by the server is compressed, and is uncompressed by the terminal (column 9, lines 8-20).

As to claim 5, Dor discloses the method of claim 1, wherein the data pre-treatment step is according to a plurality of wafers to generate corresponding wafer defect distribution data by the server and wherein the drawing pre-treatment step is according to a plurality of wafer defect distribution data to generate a corresponding drawing file by the server (column 6, lines 43-55, column 8, lines 20-25).

As to claim 6, Dor discloses the method of claim 5, wherein the network management step includes transmitting a plurality of drawing files to the terminal, and the terminal displaying the plurality of drawing files simultaneously on the displaying screen to present a plurality of distribution modes of wafer defects (column 7, line 67, column 8, line 1).

As to claim 7, Dor discloses the method of claim 1, wherein the wafer defect raw data records a position of a wafer defect relative to a chip grid, the inspection step performs defect inspection in at least two different inspection stations in sequence to generate the corresponding wafer defect raw data, and the data pre-treatment step further comprises subtracting a defect position recorded by the wafer defect raw data of a prior wafer inspection station from the wafer defect raw data corresponding to a given wafer inspection station to generate the data of a new defect in the wafer inspection

station and record the data of the new defect in the wafer defect distribution data (column 8, lines 57-67, column 9, lines 1-20).

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheela C Chawan whose telephone number is. 571-272-7446. The examiner can normally be reached on Monday - Thursday 7.30 - 6.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eileen Lillis can be reached on 571-272-6928. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheela Chawan
Patent Examiner
Group Art Unit 2624
October 8, 2007

Sheela Chawan
SHEELA CHAWAN
PRIMARY EXAMINER